DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/13/2009 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momtaz et al. (US 7088797)

With respect to claim 1, Figures 9 and 10 of Momtaz et al. disclose a synchronous memory device for synchronization of an external input clock (REFCLK) with an internal input clock (VNCLK) comprising: a Phase locked loop having a clock divider (901) comprising a plurality of clock signal dividers (911 and 912) connected in series, a power down controller (202) for determining a power down condition based at

least on a predetermined state of a clock enable signal (add or drop) that controls whether the memory device receives the external input clock and that is inputted to the loop, wherein the clock divider outputs a first clock signal (at the output of 912) being one of the output signals of the clock signal dividers excluding the last clock signal divider (912) of the series when the synchronous memory device is in the a non power down condition (Note: the power down condition is determined by the user to output a "power down signal" determined by the user when a certain sequence occurs") , wherein the clock divider (901) outputs a second clock signal (between 911 and 912) being an output signal of the last clock signal divider of the series when the synchronous memory device is in a power down condition (Note: the power down condition is determined by the user to output a "power down signal" determined by the user when a certain sequence occurs"), and wherein a frequency of the first clock signal is higher than that of the second clock signal but fails to disclose the Phase locked loop being a (DLL). It is well known in the art to include a deskew PLL on the receive side so that the clock at each data flip-flop is phased-matched to the received clock (i.e. use a DLL in the place of an PLL). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a deskew PLL on the receive side so that the clock at each data flip-flop is phase matched to the received clock for the well known purpose of eliminating delay limits in the frequency at which data can be sent.

With respect to claim 15, the circuit above produces the synchronous memory device of claim 14, wherein the frequency of the first clock signal is 2M when the

frequency of the second clock signal is M. (Note this claim is met because the dividing ratio can be selected by the user so that the first clock signal frequency is M and the second clock signal frequency is 2M (see chart in figure 10)).

Response to Arguments

4. Applicant's arguments filed 10/13/2009 have been fully considered but they are not persuasive.

With respect to applicant's argument concerning a power down condition, it is noted that any condition a circuit is in is a power down condition (i.e. not powered down or powered down).

With respect to the memory device receiving the external input clock that is inputted to the DLL, the external clock (REFCLK) is inputted into the DLL if a) the DLL consists of the entire circuit or b) if the external clock is inputted into the DLL via intervening circuits 901 and 701. Either circumstance is deemed to be a reasonable interpretation of the art.

With respect to the power down controller, the circuit add or drop does determine whether the memory device receives the external input clock.

Momtaz does disclose the clock enable signal (add or drop) and the power down circuit, because the power down circuit just has to set a condition of power down even if the condition is not active in power down or not operable. If the "power down" circuit does not claim the functionality of powering down the circuit, that aspect of the invention is not given patentable weight.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAREEM E. ALMO whose telephone number is (571)272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khareem E Almo/
Examiner, Art Unit 2816
/Lincoln Donovan/
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